What is claimed:

1. A system for despreading a PN code from a spread spectrum signal, wherein the spread spectrum signal comprises a plurality of signal samples, each signal sample having an in-phase portion and a quadrature-phase portion, and wherein the PN code comprises a plurality of chips, the system comprising:

a switch for selecting one of the in-phase portion and the quadrature-phase portion; and

a first multiplier coupled to the switch for multiplying the selected portion of one of the plurality of signal samples with one of the plurality of PN code chips to obtain a first product.

2. The system of claim 1, further comprising:

a second multiplier coupled to the switch for multiplying the selected portion of a second of the plurality of signal samples with the one of the plurality of PN code chips to obtain a second product, wherein the second of the plurality of signal samples succeeds the one of the plurality of signal samples; and

a first adder coupled to the first multiplier and the second multiplier for adding the first product with the second product to obtain a first sum.

3. The system of claim 2, further comprising:

a third multiplier coupled to the switch for multiplying the selected portion of a third of the plurality of signal samples with a second of the plurality of PN code chips to obtain a third product, wherein the third of the plurality of signal samples succeeds the second of the plurality of signal samples and wherein the second of the plurality of PN code chips succeeds the one of the plurality of PN code chips;

a fourth multiplier coupled to the switch for multiplying the selected portion of a fourth of the plurality of signal samples with the second of the plurality of PN code chips to obtain a fourth product, wherein the fourth of the plurality of signal samples succeeds the third of the plurality of signal samples;

a second adder coupled to the third multiplier and the fourth multiplier for adding the third product with the fourth product to obtain a second sum; and

a third adder coupled to the first adder and the second adder for adding the first sum with the second sum.

4. The system of claim 1, further comprising:

a second multiplier coupled to the switch for multiplying the selected portion of a second of the plurality of signal samples with a second of the plurality of PN code chips to obtain a second product, wherein the second of the plurality of signal samples succeeds the one of the plurality of signal samples and wherein the second of the plurality of PN code chips succeeds the one of the plurality of PN code chips; and

a first adder coupled to the first multiplier and the second multiplier for adding the first product with the second product to obtain a first sum.

5. The system of claim 4, further comprising:

a third multiplier coupled to the switch for multiplying the selected portion of a third of the plurality of signal samples with the second of the plurality of PN code chips to obtain a third product, wherein the third of the plurality of signal samples succeeds the second of the plurality of signal samples;

a fourth multiplier coupled to the switch for multiplying the selected portion of a fourth of the plurality of signal samples with a third of the plurality of PN code chips to obtain a fourth product, wherein the fourth of the plurality of signal samples succeeds the third of the plurality of signal samples and wherein the third of the plurality of PN code chips succeeds the second of the plurality of PN code chips;

a second adder coupled to the third multiplier and the fourth multiplier for adding the third product with the fourth product to obtain a second sum; and

a third adder coupled to the first adder and the second adder for adding the first sum with the second sum.

6. A method for despreading a PN code from a spread spectrum signal, wherein the spread spectrum signal comprises a plurality of signal samples, each signal sample having an in-phase portion and a quadrature-phase portion, and wherein the PN code comprises a plurality of chips, the method comprising:

selecting one of the in-phase portion and the quadrature-phase portion; and

multiplying the selected portion of one of the plurality of signal samples with one of the plurality of PN code chips to obtain a first product.

7. The method of claim 6, further comprising:

multiplying the selected portion of a second of the plurality of signal samples with the one of the plurality of PN code chips to obtain a second product, wherein the second of the plurality of signal samples succeeds the one of the plurality of signal samples; and

adding the first product with the second product to obtain a first sum.

8. The method of claim 7, further comprising:

multiplying the selected portion of a third of the plurality of signal samples with a second of the plurality of PN code chips to obtain a third product, wherein the third of the plurality of signal samples succeeds the second of the plurality of signal samples and wherein the second of the plurality of PN code chips succeeds the one of the plurality of PN code chips;

multiplying the selected portion of a fourth of the plurality of signal samples with the second of the plurality of PN code chips to obtain a fourth product, wherein the fourth of the plurality of signal samples succeeds the third of the plurality of signal samples;

adding the third product with the fourth product to obtain a second sum; and

adding the first sum with the second sum.

09785980-0008

9. The method of claim 6, further comprising:

multiplying the selected portion of a second of the plurality of signal samples with a second of the plurality of PN code chips to obtain a second product, wherein the second of the plurality of signal samples succeeds the one of the plurality of signal samples and wherein the second of the plurality of PN code chips succeeds the one of the plurality of PN code chips; and

adding the first product with the second product to obtain a first sum.

10. The method of claim 9, further comprising:

multiplying the selected portion of a third of the plurality of signal samples with the second of the plurality of PN code chips to obtain a third product, wherein the third of the plurality of signal samples succeeds the second of the plurality of signal samples;

multiplying the selected portion of a fourth of the plurality of signal samples with a third of the plurality of PN code chips to obtain a fourth product, wherein the fourth of the plurality of signal samples succeeds the third of the plurality of signal samples and wherein the third of the plurality of PN code chips succeeds the second of the plurality of PN code chips;

adding the third product with the fourth product to obtain a second sum; and

adding the first sum with the second sum.

09785980-0008

11. A computer data signal embodied in a carrier wave comprising:

(a) a receiving source code segment comprising means for receiving a spread spectrum signal, wherein the spread spectrum signal comprises a plurality of signal samples, each signal sample having an in-phase portion and a quadrature-phase portion; and

(b) a processing source code segment comprising:

(i) means for selecting one of the in-phase portion and the quadrature-phase portion; and

(ii) means for multiplying the selected portion of one of the plurality of signal samples with one of a plurality of PN code chips to obtain a first product.

12. The computer data signal of claim 11, wherein the processing source code segment further comprises:

(iii) means for multiplying the selected portion of a second of the plurality of signal samples with the one of the plurality of PN code chips to obtain a second product, wherein the second of the plurality of signal samples succeeds the one of the plurality of signal samples; and

(iv) means for adding the first product with the second product to obtain a first sum.

13. The computer data signal of claim 12, wherein the processing source code segment further comprises:

(v) means for multiplying the selected portion of a third of the plurality of signal samples with a second of the plurality of PN code chips to obtain a third product, wherein the third of the plurality of signal samples succeeds the second of the plurality of signal samples and wherein the second of the plurality of PN code chips succeeds the one of the plurality of PN code chips;

(vi) means for multiplying the selected portion of a fourth of the plurality of signal samples with the second of the plurality of PN code chips to obtain a fourth product, wherein the fourth of the plurality of signal samples succeeds the third of the plurality of signal samples;

(vii) means for adding the third product with the fourth product to obtain a second sum; and

(viii) means for adding the first sum with the second sum.

09785980-0008

14. The computer data signal of claim 11, wherein the processing source code segment further comprises:

(iii) means for multiplying the selected portion of a second of the plurality of signal samples with a second of the plurality of PN code chips to obtain a second product, wherein the second of the plurality of signal samples succeeds the one of the plurality of signal samples and wherein the second of the plurality of PN code chips succeeds the one of the plurality of PN code chips; and

(iv) means for adding the first product with the second product to obtain a first sum.

15. The computer data signal of claim 14, wherein the processing source code segment further comprises:

(v) means for multiplying the selected portion of a third of the plurality of signal samples with the second of the plurality of PN code chips to obtain a third product, wherein the third of the plurality of signal samples succeeds the second of the plurality of signal samples;

(vi) means for multiplying the selected portion of a fourth of the plurality of signal samples with a third of the plurality of PN code chips to obtain a fourth product, wherein the fourth of the plurality of signal samples succeeds the third of the plurality of signal samples and wherein the third of the plurality of PN code chips succeeds the second of the plurality of PN code chips;

(vii) means for adding the third product with the fourth product to obtain a second sum; and

(viii) means for adding the first sum with the second sum.

16. A computer readable medium having software for despreading a PN code from a spread spectrum signal, wherein the spread spectrum signal comprises a plurality of signal samples, each signal sample having an in-phase portion and a quadrature-phase portion, and wherein the PN code comprises a plurality of chips, the computer readable medium comprising:

means for selecting one of the in-phase portion and the quadrature-phase portion; and

means for multiplying the selected portion of one of the plurality of signal samples with one of the plurality of PN code chips to obtain a first product.

17. The computer readable medium of claim 16, further comprising:

means for multiplying the selected portion of a second of the plurality of signal samples with the one of the plurality of PN code chips to obtain a second product, wherein the second of the plurality of signal samples succeeds the one of the plurality of signal samples; and

means for adding the first product with the second product to obtain a first sum.

09785980-0008

18. The computer readable medium of claim 17, further comprising:

means for multiplying the selected portion of a third of the plurality of signal samples with a second of the plurality of PN code chips to obtain a third product, wherein the third of the plurality of signal samples succeeds the second of the plurality of signal samples and wherein the second of the plurality of PN code chips succeeds the one of the plurality of PN code chips;

means for multiplying the selected portion of a fourth of the plurality of signal samples with the second of the plurality of PN code chips to obtain a fourth product, wherein the fourth of the plurality of signal samples succeeds the third of the plurality of signal samples;

means for adding the third product with the fourth product to obtain a second sum; and

means for adding the first sum with the second sum.

19. The computer readable medium of claim 16, further comprising:

means for multiplying the selected portion of a second of the plurality of signal samples with a second of the plurality of PN code chips to obtain a second product, wherein the second of the plurality of signal samples succeeds the one of the plurality of signal samples and wherein the second of the plurality of PN code chips succeeds the one of the plurality of PN code chips; and

means for adding the first product with the second product to obtain a first sum.

20. The computer readable medium of claim 19, further comprising:

means for multiplying the selected portion of a third of the plurality of signal samples with the second of the plurality of PN code chips to obtain a third product, wherein the third of the plurality of signal samples succeeds the second of the plurality of signal samples;

means for multiplying the selected portion of a fourth of the plurality of signal samples with a third of the plurality of PN code chips to obtain a fourth product, wherein the fourth of the plurality of signal samples succeeds the third of the plurality of signal samples and wherein the third of the plurality of PN code chips succeeds the second of the plurality of PN code chips;

means for adding the third product with the fourth product to obtain a second sum; and

means for adding the first sum with the second sum.

09604595.062700

21. A system for despreading a PN code from a spread spectrum signal, wherein the spread spectrum signal comprises a plurality of signal sample pairs, each pair comprising an even signal sample and an odd signal sample, each signal sample having an in-phase portion and a quadrature-phase portion, and wherein the PN code comprises a plurality of chips, the system comprising:

a first switch for selecting one of the in-phase portion and the quadrature-phase portion;

a second switch coupled to the first switch for selecting one of the even sample and the odd sample; and

a first multiplier coupled to the second switch for multiplying the selected portion of the selected sample of one of the plurality of signal sample pairs with one of the plurality of PN code chips to obtain a first product.

22. The system of claim 21, further comprising:

a second multiplier coupled to the second switch for multiplying the selected portion of the selected sample of a second of the plurality of signal sample pairs with a second of the plurality of PN code chips to obtain a second product, wherein the second of the plurality of signal sample pairs succeeds the one of the plurality of signal sample pairs, and the second of the plurality of PN code chips succeeds the one of the plurality of PN code chips; and

an adder coupled to the first multiplier and the second multiplier for adding the first product with the second product to obtain a first sum.

23. The system of claim 22, further comprising:

a third multiplier coupled to the second switch for multiplying the selected portion of the other sample of the one of the plurality of signal sample pairs with the one of the plurality of PN code chips to obtain a third product;

a fourth multiplier coupled to the second switch for multiplying the selected portion of the other sample of the second of the plurality of signal sample pairs with the second of the plurality of PN code chips to obtain a fourth product;

a second adder coupled to the third multiplier and the fourth multiplier for adding the third product with the fourth product to obtain a second sum; and

a third adder coupled to the first adder and the second adder for adding the first sum with the second sum.

24. The system of claim 22, further comprising:

a third multiplier coupled to the second switch for multiplying the selected portion of the other sample of the one of the plurality of signal sample pairs with the second of the plurality of PN code chips to obtain a third product;

a fourth multiplier coupled to the second switch for multiplying the selected portion of the other sample of the second of the plurality of signal sample pairs with a third of the plurality of PN code chips to obtain a fourth product, wherein the third of the plurality of PN code chips succeeds the second of the plurality of PN code chips;

a second adder coupled to the third multiplier and the fourth multiplier for adding the third product with the fourth product to obtain a second sum; and

a third adder coupled to the first adder and the second adder for adding the first sum with the second sum.

25. A method for despreading a PN code from a spread spectrum signal, wherein the spread spectrum signal comprises a plurality of signal sample pairs, each pair comprising an even signal sample and an odd signal sample, each signal sample having an in-phase portion and a quadrature-phase portion, and wherein the PN code comprises a plurality of chips, the method comprising:

selecting one of the in-phase portion and the quadrature-phase portion;

selecting one of the even sample and the odd sample; and

multiplying the selected portion of the selected sample of one of the plurality of signal sample pairs with one of the plurality of PN code chips to obtain a first product.

26. The method of claim 25, further comprising:

multiplying the selected portion of the selected sample of a second of the plurality of signal sample pairs with a second of the plurality of PN code chips to obtain a second product, wherein the second of the plurality of signal sample pairs succeeds the one of the plurality of signal sample pairs, and the second of the plurality of PN code chips succeeds the one of the plurality of PN code chips; and

adding the first product with the second product to obtain a first sum.

27. The method of claim 26, further comprising:

multiplying the selected portion of the other sample of the one of the plurality of signal sample pairs with the one of the plurality of PN code chips to obtain a third product;

multiplying the selected portion of the other sample of the second of the plurality of signal sample pairs with the second of the plurality of PN code chips to obtain a fourth product;

adding third product with the fourth product to obtain a second sum; and

adding the first sum with the second sum.

28. The method of claim 26, further comprising:

multiplying the selected portion of the other sample of the one of the plurality of signal sample pairs with the second of the plurality of PN code chips to obtain a third product;

multiplying the selected portion of the other sample of the second of the plurality of signal sample pairs with a third of the plurality of PN code chips to obtain a fourth product, wherein the third of the plurality of PN code chips succeeds the second of the plurality of PN code chips;

adding third product with the fourth product to obtain a second sum; and

adding the first sum with the second sum.

29. A computer data signal embodied in a carrier wave comprising:

(a) a receiving source code segment comprising means for receiving a spread spectrum signal, wherein the spread spectrum signal comprises a plurality of signal sample pairs, each pair comprising an even signal sample and an odd signal sample, each signal sample having an in-phase portion and a quadrature-phase portion; and

(b) a processing source code segment comprising:

(i) means for selecting one of the in-phase portion and the quadrature-phase portion;

(ii) means for selecting one of the even sample and the odd sample; and

(iii) means for multiplying the selected portion of the selected sample of one of the plurality of signal sample pairs with one of a plurality of PN code chips to obtain a first product.

30. The computer data signal of claim 29, wherein the processing source code segment further comprises:

(iv) means for multiplying the selected portion of the selected sample of a second of the plurality of signal sample pairs with a second of the plurality of PN code chips to obtain a second product, wherein the second of the plurality of signal sample pairs succeeds the one of the plurality of signal sample pairs, and the second of the plurality of PN code chips succeeds the one of the plurality of PN code chips; and

(v) means for adding the first product with the second product to obtain a first sum.

31. The computer data signal of claim 30, wherein the processing source code segment further comprises:

(vi) means for multiplying the selected portion of the other sample of the one of the plurality of signal sample pairs with the one of the plurality of PN code chips to obtain a third product;

(vii) means for multiplying the selected portion of the other sample of the second of the plurality of signal sample pairs with the second of the plurality of PN code chips to obtain a fourth product;

(viii) means for adding the third product with the fourth product to obtain a second sum; and

(ix) means for adding the first sum with the second sum.

32. The computer data signal of claim 30, wherein the processing source code segment further comprises:

(vi) means for multiplying the selected portion of the other sample of the one of the plurality of signal sample pairs with the second of the plurality of PN code chips to obtain a third product;

(vii) means for multiplying the selected portion of the other sample of the second of the plurality of signal sample pairs with a third of the plurality of PN code chips to obtain a fourth product, wherein the third of the plurality of PN code chips succeeds the second of the plurality of PN code chips;

(viii) means for adding the third product with the fourth product to obtain a second sum; and

(ix) means for adding the first sum with the second sum.

33. A computer readable medium having software for despreading a PN code from a spread spectrum signal, wherein the spread spectrum signal comprises a plurality of signal sample pairs, each pair comprising an even signal sample and an odd signal sample, each signal sample having an in-phase portion and a quadrature-phase portion, and wherein the PN code comprises a plurality of chips, the computer readable medium comprising:

means for selecting one of the in-phase portion and the quadrature-phase portion;

means for selecting one of the even sample and the odd sample; and

means for multiplying the selected portion of the selected sample of one of the plurality of signal sample pairs with one of the plurality of PN code chips to obtain a first product.

34. The computer readable medium of claim 33, further comprising:

means for multiplying the selected portion of the selected sample of a second of the plurality of signal sample pairs with a second of the plurality of PN code chips to obtain a second product, wherein the second of the plurality of signal sample pairs succeeds the one of the plurality of signal sample pairs, and the second of the plurality of PN code chips succeeds the one of the plurality of PN code chips; and

means for adding the first product with the second product to obtain a first sum.

35. The computer readable medium of claim 34, further comprising:

means for multiplying the selected portion of the other sample of the one of the plurality of signal sample pairs with the one of the plurality of PN code chips to obtain a third product;

means for multiplying the selected portion of the other sample of the second of the plurality of signal sample pairs with the second of the plurality of PN code chips to obtain a fourth product;

means for adding the third product with the fourth product to obtain a second sum; and

means for adding the first sum with the second sum.

36. The computer readable medium of claim 34, further comprising:

means for multiplying the selected portion of the other sample of the one of the plurality of signal sample pairs with the second of the plurality of PN code chips to obtain a third product;

means for multiplying the selected portion of the other sample of the second of the plurality of signal sample pairs with a third of the plurality of PN code chips to obtain a fourth product, wherein the third of the plurality of PN code chips succeeds the second of the plurality of PN code chips;

means for adding the third product with the fourth product to obtain a second sum; and

means for adding the first sum with the second sum.

09785980-0008

37. A system for processing communication data from a code signal input, wherein the code signal input comprises a plurality of chips, the system comprising:

a signal sampler operable to receive signal data, wherein the signal data comprises a plurality of signal samples, each signal sample having an in-phase portion and a quadrature-phase portion;

a Doppler shift system operable to provide a Doppler shift correction value; and

a time domain signal processor in signal communication with the signal sampler, the Doppler shift system and the code signal input, the time domain signal processor operable to:

shift the signal data by the Doppler shift correction value;

select one of the in-phase portion and the quadrature-phase portion; and

multiply the selected portion of one of the plurality of Doppler-shifted signal samples with one of the plurality of chips.

38. A method for processing communication data comprising:

receiving signal data, wherein the signal data comprises a plurality of signal samples, each signal sample having an in-phase portion and a quadrature-phase portion;

applying a Doppler shift correction value to the signal data;

receiving a code signal, wherein the code signal comprises a plurality of chips;

selecting one of the in-phase portion and the quadrature-phase portion; and

multiplying the selected portion of one of the plurality of Doppler-shifted signal samples with one of the plurality of chips.

DOCKET: 09785980-0008

39. A system for processing radio frequency data comprising:

a signal sample receiver operable to receive signal data, wherein the signal data comprises a plurality of signal samples, each signal sample having an in-phase portion and a quadrature-phase portion;

a Doppler shift corrector operable to provide a Doppler shift correction value;

a code signal receiver operable to receive a code signal, wherein the code signal comprises a plurality of chips;

a processor coupled to the signal sample receiver, the Doppler shift corrector, and the code signal receiver, the processor operable to:

apply the Doppler shift correction value to the signal data;

select one of the in-phase portion and the quadrature-phase portion; and

o multiply the selected portion of one of the plurality of Doppler-shifted signal samples with one of the plurality of chips; and

a signal processor coupled to the signal sample receiver, the signal processor operable to process the signal data to extract encoded data.

09785980-0008

40. A system for processing communication data from a code signal input, wherein the code signal input comprises a plurality of chips, the system comprising:

means for receiving signal data, wherein the signal data comprises a plurality of signal samples, each signal sample having an in-phase portion and a quadrature-phase portion;

means for providing a Doppler shift correction value; and

a time domain signal processor coupled to the receiving means, providing means and the code signal input, the time domain signal processor operable to:

shift the signal data by the Doppler shift correction value;

select one of the in-phase portion and the quadrature-phase portion; and

multiply the selected portion of one of the plurality of Doppler-shifted signal samples with one of the plurality of chips.

09554055.062700

41. A computer data signal embodied in a carrier wave comprising:

(a) a receiving source code segment comprising means for receiving signal data, wherein the signal data comprises a plurality of signal samples, each signal sample having an in-phase portion and a quadrature-phase portion; and

(b) a processing source code segment comprising:

(i) means for providing a Doppler shift correction value; and

(ii) means for processing coupled to the receiving means, providing means and the code signal input, the processing means operable to:

(1) shift the signal data by the Doppler shift correction value;

(2) select one of the in-phase portion and the quadrature-phase portion; and

(3) multiply the selected portion of one of the plurality of Doppler-shifted signal samples with one of a plurality of coded signal chips.

09785980-0008

42. A computer data signal embodied in a carrier wave comprising:

(a) a receiving source code segment comprising means for receiving signal data, wherein the signal data comprises a plurality of signal samples, each signal sample having an in-phase portion and a quadrature-phase portion; and

(b) a processing source code segment comprising:

(i) means for applying a Doppler shift correction value to the signal data,

(ii) means for receiving a code signal, wherein the code signal comprises a plurality of chips,

(iii) means for selecting one of the in-phase portion and the quadrature-phase portion; and

(iv) means for multiply the selected portion of one of the plurality of Doppler-shifted signal samples with one of the plurality of chips.

43. A computer readable medium having software for processing communication data from a code signal, the computer readable medium comprising:

logic configured for receiving signal data, wherein the signal data comprises a plurality of signal samples, each signal sample having an in-phase portion and a quadrature-phase portion;

logic configured for applying a Doppler shift correction value to the signal data;

logic configured for receiving the code signal, wherein the code signal comprises a plurality of chips;

logic configured for selecting one of the in-phase portion and the quadrature-phase portion; and

logic configured for multiply the selected portion of one of the plurality of Doppler-shifted signal samples with one of the plurality of chips.

09785980-0008

44. A system for processing communication data from a code signal input, wherein the code signal input comprises a plurality of chips, the system comprising:

a signal sampler operable to receive signal data, wherein the signal data comprises a plurality of signal sample pairs, each pair comprising an even signal sample and an odd signal sample, each signal sample having an in-phase portion and a quadrature-phase portion;

a Doppler shift system operable to provide a Doppler shift correction value; and

a time domain signal processor in signal communication with the signal sampler, the Doppler shift system and the code signal input, the time domain signal processor operable to:

shift the signal data by the Doppler shift correction value;

select one of the in-phase portion and the quadrature-phase portion;

select one of the even sample and the odd sample; and

multiply the selected portion of the selected sample of one of the plurality of Doppler-shifted signal sample pairs with one of the plurality of PN code chips.

09785980-0008

45. A method for processing communication data comprising:

receiving signal data, wherein the signal data comprises a plurality of signal sample pairs, each pair comprising an even signal sample and an odd signal sample, each signal sample having an in-phase portion and a quadrature-phase portion;

applying a Doppler shift correction value to the signal data;

receiving a code signal, wherein the code signal comprises a plurality of chips;

selecting one of the in-phase portion and the quadrature-phase portion;

selecting one of the even sample and the odd sample; and

multiplying the selected portion of the selected sample of one of the plurality of Doppler-shifted signal sample pairs with one of the plurality of PN code chips.

09785980.0008

46. A system for processing radio frequency data comprising:

a signal sample receiver operable to receive signal data, wherein the signal data comprises a plurality of signal sample pairs, each pair comprising an even signal sample and an odd signal sample, each signal sample having an in-phase portion and a quadrature-phase portion;

a Doppler shift corrector operable to provide a Doppler shift correction value;

a code signal receiver operable to receive a code signal, wherein the code signal comprises a plurality of chips;

a processor coupled to the signal sample receiver, the Doppler shift corrector, and the code signal receiver, the processor operable to:

apply the Doppler shift correction value to the signal data;

select one of the in-phase portion and the quadrature-phase portion;

select one of the even sample and the odd sample; and

multiply the selected portion of the selected sample of one of the plurality of Doppler-shifted signal sample pairs with one of the plurality of PN code chips; and

a signal processor coupled to the signal sample receiver, the signal processor operable to process the signal data to extract encoded data.

0500450.020204

47. A system for processing communication data from a code signal input, wherein the code signal input comprises a plurality of chips, the system comprising:

means for receiving signal data, wherein the signal data comprises a plurality of signal sample pairs, each pair comprising an even signal sample and an odd signal sample, each signal sample having an in-phase portion and a quadrature-phase portion;

means for providing a Doppler shift correction value; and

a time domain signal processor coupled to the receiving means, providing means and the code signal input, the time domain signal processor operable to:

shift the signal data by the Doppler shift correction value;

select one of the in-phase portion and the quadrature-phase portion; and

multiply the selected portion of one of the plurality of Doppler-shifted signal samples with one of the plurality of chips.

48. A computer data signal embodied in a carrier wave comprising:

(a) a receiving source code segment comprising means for receiving signal data, wherein the signal data comprises a plurality of signal sample pairs, each pair comprising an even signal sample and an odd signal sample, each signal sample having an in-phase portion and a quadrature-phase portion; and

(b) a processing source code segment comprising:

(i) means for providing a Doppler shift correction value; and

(ii) means for processing coupled to the receiving means, providing means and the code signal input, the processing means operable to:

(1) shift the signal data by the Doppler shift correction value;

(2) select one of the in-phase portion and the quadrature-phase portion;

(3) select one of the even sample and the odd sample; and

(4) multiply the selected portion of the selected sample of one of the plurality of Doppler-shifted signal sample pairs with one of a plurality of PN code chips.

49. A computer data signal embodied in a carrier wave comprising:

(a) a receiving source code segment comprising means for receiving signal data, wherein the signal data comprises a plurality of signal sample pairs, each pair comprising an even signal sample and an odd signal sample, each signal sample having an in-phase portion and a quadrature-phase portion; and

(b) a processing source code segment comprising:

(i) means for applying a Doppler shift correction value to the signal data,

(ii) means for receiving a code signal, wherein the code signal comprises a plurality of chips,

(iii) means for selecting one of the in-phase portion and the quadrature-phase portion;

(iv) means for selecting one of the even sample and the odd sample; and

(v) means for multiplying the selected portion of the selected sample of one of the plurality of Doppler-shifted signal sample pairs with one of the plurality of PN code chips.

50. A computer readable medium having software for processing communication data from a code signal, the computer readable medium comprising:

logic configured to receive signal data, wherein the signal data comprises a plurality of signal samples, each signal sample having an in-phase portion and a quadrature-phase portion;

logic configured to apply a Doppler shift correction value to the signal data;

logic configured to receive the code signal, wherein the code signal comprises a plurality of chips;

logic configured to select one of the in-phase portion and the quadrature-phase portion;

logic configured to multiply the selected portion of one of the plurality of Doppler-shifted signal samples with one of the plurality of PN code chips.

51. A computer readable medium having software for processing communication data from a code signal, the computer readable medium comprising:

logic configured to receive signal data, wherein the signal data comprises a plurality of signal sample pairs, each pair comprising an even signal sample and an odd signal sample, each signal sample having an in-phase portion and a quadrature-phase portion;

logic configured to apply a Doppler shift correction value to the signal data;

logic configured to receive the code signal, wherein the code signal comprises a plurality of chips;

logic configured to select one of the in-phase portion and the quadrature-phase portion;

logic configured to select one of the even sample and the odd sample; and

logic configured to multiply the selected portion of the selected sample of one of the plurality of Doppler-shifted signal sample pairs with one of the plurality of PN code chips.

02/20/00 15:24:26

52. A method for measuring time related to satellite data messages for use with a satellite positioning system (SPS), the method comprising:

receiving in a mobile SPS receiver at least a portion of a satellite data message;

determining a first record of the at least a portion of the satellite data message by despreading a PN code from the satellite data message, wherein the satellite data message comprises a plurality of signal samples, each signal sample having an in-phase portion and a quadrature-phase portion, and wherein the PN code comprises a plurality of chips, the despreading step comprising:

selecting one of the in-phase portion and the quadrature-phase portion; and

multiplying the selected portion of one of the plurality of signal samples with one of the plurality of PN code chips; and

transmitting from the mobile SPS receiver the first record to a remote basestation for the purpose of determining a time indicating when the first record was received at the mobile SPS receiver.

53. A method for measuring time related to satellite data messages for use with a satellite positioning system (SPS), the method comprising:

receiving in a mobile SPS receiver at least a portion of a satellite data message;

determining a first record of the at least a portion of the satellite data message by despreading a PN code from the satellite data message, wherein the satellite data message comprises a plurality of signal sample pairs, each pair comprising an even signal sample and an odd signal sample, each signal sample having an in-phase portion and a quadrature-phase portion, and wherein the PN code comprises a plurality of chips, the despreading step comprising:

selecting one of the in-phase portion and the quadrature-phase portion;

selecting one of the even sample and the odd sample; and

multiplying the selected portion of the selected sample of one of the plurality of signal sample pairs with one of the plurality of PN code chips; and

transmitting from the mobile SPS receiver the first record to a remote basestation for the purpose of determining a time indicating when the first record was received at the mobile SPS receiver.

09785980-0008

54. A satellite positioning system (SPS) receiver comprising:

an antenna for receiving SPS signals;

a demodulator coupled to the antenna, the demodulator removing a PN code from the SPS signals, wherein each SPS signal comprises a plurality of signal samples, each signal sample having an in-phase portion and a quadrature-phase portion and wherein the PN code comprises a plurality of chips, the demodulator comprising:

a switch for selecting one of the in-phase portion and the quadrature-phase portion; and

a first multiplier coupled to the switch for multiplying the selected portion of one of the plurality of signal samples with one of the plurality of PN code chips;

a processor coupled to the demodulator, the processor determining a first record of at least a portion of a satellite data message received from the demodulator; and

a transmitter coupled to the processor, the transmitter transmitting the first record to a remote basestation for the purpose of determining a time indicating when the first record was received at the SPS receiver.

09785980-0008 Docket No. 97RSS501CIP2

55. A satellite positioning system (SPS) receiver comprising:

an antenna for receiving SPS signals;

a demodulator coupled to the antenna, the demodulator removing a PN code from the SPS signals, wherein each SPS signal comprises a plurality of signal sample pairs, each pair comprising an even signal sample and an odd signal sample, each signal sample having an in-phase portion and a quadrature-phase portion, and wherein the PN code comprises a plurality of chips, the demodulator comprising:

a first switch for selecting one of the in-phase portion and the quadrature-phase portion;

a second switch coupled to the first switch for selecting one of the even sample and the odd sample; and

a first multiplier coupled to the second switch for multiplying the selected portion of the selected sample of one of the plurality of signal sample pairs with one of the plurality of PN code chips;

a processor coupled to the demodulator, the processor determining a first record of at least a portion of a satellite data message received from the demodulator; and

a transmitter coupled to the processor, the transmitter transmitting the first record to a remote basestation for the purpose of determining a time indicating when the first record was received at the SPS receiver.

56. A satellite positioning system (SPS) receiver comprising:

a SPS antenna for receiving SPS signals;

a digitizer coupled to the SPS antenna;

a digital memory coupled to the digitizer, the digital memory storing a digital representation of the SPS signals;

a digital processor coupled to the digital memory, the digital processor processing the SPS signals and determining at least one pseudorange from the SPS signals, the digital processor removing a PN code from the SPS signals to provide a first record of at least a portion of a satellite data message in the SPS signals, wherein each SPS signal comprises a plurality of signal samples, each signal sample having an in-phase portion and a quadrature-phase portion, and wherein the PN code comprises a plurality of chips, the digital processor comprising:

a switch for selecting one of the in-phase portion and the quadrature-phase portion; and

a first multiplier coupled to the switch for multiplying the selected portion of one of the plurality of signal samples with one of the plurality of PN code chips; and

a transmitter coupled to the digital processor, the transmitter transmitting the first record to a remote basestation.

57. A satellite positioning system (SPS) receiver comprising:

a SPS antenna for receiving SPS signals;

a digitizer coupled to the SPS antenna;

a digital memory coupled to the digitizer, the digital memory storing a digital representation of the SPS signals;

a digital processor coupled to the digital memory, the digital processor processing the SPS signals and determining at least one pseudorange from the SPS signals, the digital processor removing a PN code from the SPS signals to provide a first record of at least a portion of a satellite data message in the SPS signals, wherein each SPS signal comprises a plurality of signal sample pairs, each pair comprising an even signal sample and an odd signal sample, each signal sample having an in-phase portion and a quadrature-phase portion, and wherein the PN code comprises a plurality of chips, the digital processor comprising:

a first switch for selecting one of the in-phase portion and the quadrature-phase portion;

a second switch coupled to the first switch for selecting one of the even sample and the odd sample; and

a first multiplier coupled to the second switch for multiplying the selected portion of the selected sample of one of the plurality of signal sample pairs with one of the plurality of PN code chips; and

a transmitter coupled to the digital processor, the transmitter transmitting the first record to a remote basestation.

58. A system of a mobile satellite positioning system (SPS) receiver and a basestation remotely positioned relative to the mobile SPS receiver, the system comprising:

the mobile SPS receiver comprising:

an antenna for receiving SPS signals;

a processor coupled to the antenna, the processor despreading a PN code from the SPS signals to determine a first record of at least a portion of a satellite data message in the SPS signals, wherein each SPS signal comprises a plurality of signal samples, each signal sample having an in-phase portion and a quadrature-phase portion, and wherein the PN code comprises a plurality of chips, the processor comprising:

a switch for selecting one of the in-phase portion and the quadrature-phase portion; and

a first multiplier coupled to the switch for multiplying the selected portion of one of the plurality of signal samples with one of the plurality of PN code chips;

a transmitter coupled to the processor, the transmitter transmitting the first record to the basestation;

the basestation comprising:

a receiver for receiving the first record;

a data processor coupled to the receiver, the data processor performing a comparison of the first record with a second record of the satellite data message, wherein the first record and the second record overlap at least partially in time, the data processor determining a time from the comparison, the time indicating when the first record was received at the mobile SPS receiver.

59. A system of a mobile satellite positioning system (SPS) receiver and a basestation remotely positioned relative to the mobile SPS receiver, the system comprising:

the mobile SPS receiver comprising:

an antenna for receiving SPS signals;

a processor coupled to the antenna, the processor despreading a PN code from the SPS signals to determine a first record of at least a portion of a satellite data message in the SPS signals, wherein each SPS signal comprises a plurality of signal sample pairs, each pair comprising an even signal sample and an odd signal sample, each signal sample having an in-phase portion and a quadrature-phase portion, and wherein the PN code comprises a plurality of chips, the processor comprising:

a first switch for selecting one of the in-phase portion and the quadrature-phase portion;

a second switch coupled to the first switch for selecting one of the even sample and the odd sample; and

a first multiplier coupled to the second switch for multiplying the selected portion of the selected sample of one of the plurality of signal sample pairs with one of the plurality of PN code chips

a transmitter coupled to the processor, the transmitter transmitting the first record to the basestation;

the basestation comprising:

a receiver for receiving the first record;

a data processor coupled to the receiver, the data processor performing a comparison of the first record with a second record of the satellite data message, wherein the first record and the second record overlap at least partially in time, the data processor determining a time

from the comparison, the time indicating when the first record was received at the mobile SPS receiver.

60. A mobile satellite positioning system (SPS) receiver comprising:

an antenna for receiving SPS signals;

a demodulator coupled to the antenna, the demodulator removing a PN code from the SPS signals, wherein each SPS signal comprises a plurality of signal samples, each signal sample having an in-phase portion and a quadrature-phase portion and wherein the PN code comprises a plurality of chips, the demodulator comprising:

a switch for selecting one of the in-phase portion and the quadrature-phase portion; and

a first multiplier coupled to the switch for multiplying the selected portion of one of the plurality of signal samples with one of the plurality of PN code chips;

a processor coupled to the demodulator, the processor determining a first record of at least a portion of a satellite data message received from the demodulator;

a communication antenna;

a communication receiver coupled to the communication antenna and to the processor, the communication receiver receiving a second record of the satellite data message, wherein the first record and the second record overlap at least partially in time, the processor comparing the first record and the second record and determining a time indicating when the first record was received.

09785980-0008

61. A mobile satellite positioning system (SPS) receiver comprising:

an antenna for receiving SPS signals;

a demodulator coupled to the antenna, the demodulator removing a PN code from the SPS signals, wherein each SPS signal comprises a plurality of signal sample pairs, each pair comprising an even signal sample and an odd signal sample, each signal sample having an in-phase portion and a quadrature-phase portion, and wherein the PN code comprises a plurality of chips, the demodulator comprising:

a first switch for selecting one of the in-phase portion and the quadrature-phase portion;

a second switch coupled to the first switch for selecting one of the even sample and the odd sample; and

a first multiplier coupled to the second switch for multiplying the selected portion of the selected sample of one of the plurality of signal sample pairs with one of the plurality of PN code chips;

a processor coupled to the demodulator, the processor determining a first record of at least a portion of a satellite data message received from the demodulator;

a communication antenna;

a communication receiver coupled to the communication antenna and to the processor, the communication receiver receiving a second record of the satellite data message, wherein the first record and the second record overlap at least partially in time, the processor comparing the first record and the second record and determining a time indicating when the first record was received.

62. A method of controlling a communication link and processing data representative of GPS signals from at least one satellite in a GPS receiver, the method comprising:

processing the data representative of GPS signals from at least one satellite in a processing unit, including performing a correlation function to determine a pseudorange based on the data representative of GPS signals, wherein the data representative of GPS signals comprises a plurality of signal samples, each signal sample having an in-phase portion and a quadrature-phase portion, the performing a correlation function step comprising:

selecting one of the in-phase portion and the quadrature-phase portion; and

multiplying the selected portion of one of the plurality of signal samples with one of a plurality of PN code chips;

controlling communication signals through the communication link by using the processing unit to perform the controlling and wherein the processing unit performs demodulation of communication signals sent to the GPS receiver.

09785980-0008

63. A method of controlling a communication link and processing data representative of GPS signals from at least one satellite in a GPS receiver, the method comprising:

processing the data representative of GPS signals from at least one satellite in a processing unit, including performing a correlation function to determine a pseudorange based on the data representative of GPS signals, wherein the data representative of GPS signals comprises a plurality of signal sample pairs, each pair comprising an even signal sample and an odd signal sample, each signal sample having an in-phase portion and a quadrature-phase portion, the performing a correlation function step comprising:

selecting one of the in-phase portion and the quadrature-phase portion;

selecting one of the even sample and the odd sample; and

multiplying the selected portion of the selected sample of one of the plurality of signal sample pairs with one of a plurality of PN code chips; and

controlling communication signals through the communication link by using the processing unit to perform the controlling and wherein the processing unit performs demodulation of communication signals sent to the GPS receiver.

64. A GPS receiver comprising:

a GPS antenna for receiving data representative of GPS signals from at least one satellite;

a digital processor coupled to the GPS antenna, the digital processor processing the data representative of GPS signals from at least one satellite, including performing a matched filtering operation to determine a pseudorange based on the data representative of GPS signals, wherein the data representative of GPS signals comprises a plurality of signal samples, each signal sample having an in-phase portion and a quadrature-phase portion, the matched filter operation comprising:

a switch for selecting one of the in-phase portion and the quadrature-phase portion; and

a first multiplier coupled to the switch for multiplying the selected portion of one of the plurality of signal samples with one of a plurality of PN code chips;

the digital processor also processing communication signals received through a communication link, the processing of communication signals comprising demodulation of communication signals sent to the GPS receiver.

65. A GPS receiver comprising:

a GPS antenna for receiving data representative of GPS signals from at least one satellite;

a digital processor coupled to the GPS antenna, the digital processor processing the data representative of GPS signals from at least one satellite, including performing a matched filtering operation to determine a pseudorange based on the data representative of GPS signals, wherein the data representative of GPS signals comprises a plurality of signal sample pairs, each pair comprising an even signal sample and an odd signal sample, each signal sample having an in-phase portion and a quadrature-phase portion, the matched filter operation comprising:

a first switch for selecting one of the in-phase portion and the quadrature-phase portion;

a second switch coupled to the first switch for selecting one of the even sample and the odd sample; and

a first multiplier coupled to the second switch for multiplying the selected portion of the selected sample of one of the plurality of signal sample pairs with one of the plurality of PN code chips;

the digital processor also processing communication signals received through a communication link, the processing of communication signals comprising demodulation of communication signals sent to the GPS receiver.

09785980-0008